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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,940	09/09/2003	Steven M. Eustis	BUR920030049US1 (16664)	3095

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EXAMINER	
WASHBURN, DOUGLAS N	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,940	EUSTIS ET AL.	
	Examiner	Art Unit	
	Douglas N Washburn	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 11-13* is/are allowed.

6)☒ Claim(s) *1,3-10 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09 September 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1 Claims 2 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-10, and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Schwarz (US 6,795,942) (Hereafter referred to as Schwarz).

Schwarz teaches:

Performing first and second passes of self-test on a RAM memory in regard to claim 1

(e.g.; column 4, lines66 et seq; column 5, lines 1-3);

In a first pass of self-test, determining a worst failing column of the RAM memory in regard to claim 1

(e.g.; column 5, lines 15-20);

After completion of a first pass of self-test, allocating a spare column to replace the worst failing column in regard to claim 1

(e.g.; column 5, lines 44-57);

In a second pass of self-test, determining unique failing row addresses in a memory in regard to claim 1

(e.g.; column 6, lines 8-9; column 8, lines 37-41);

After completion of a second pass of self-test, allocating spare rows to replace failing rows in regard to claim 1

(e.g.; column 5, lines 61-65);

Testing one column at a time while counting the number of unique failing row addresses of the tested column by masking all columns except the tested column, such that only the un-masked tested column can produce an error in a data-out comparator in regard to claim 3

(e.g.; column 5, lines 4-14; column 6, lines 61-65);

A decoder is used to mask all columns except a tested column in regard to claim 4

(e.g.; column 9, lines 26-28; figure 3, elements 80, 82 and 84);

During a first pass of self-test a Built-In Self Test (BIST) generates a column address signal designating a particular column in memory to be selected and tested, which is input to a decoder to select the particular column to be tested, and during normal operation of the RAM a stored worst column address signal is decoded by decoder to implement redundant data column in place of the worst tested column in regard to claim 5

(e.g.; column 5, lines 4-20);

A pass/fail signal from a data-out comparator is used to enable a Failing Address Register (FAR) to store each unique failing row address in regard to claim 6

(e.g.; column 9, lines 61-63; figure 3);

As each unique failing row address is stored, a counter is enabled to count the number of unique failing row addresses for an unmasked column, and at the end of testing of the unmasked column, if the error count value for the unmasked column exceeds a previously stored high error count value from previously tested columns, then the unmasked column is determined to be the worst column so far, and the error count value for the unmasked column is stored in an error count register, and a bit-address for the unmasked column is stored in a repair register in regard to claim 7

(e.g.; column 7, lines 13-65);

After completion of a first pass of self-test, a stored bit address stored in a repair register is used to enable a spare column, prior to a second pass of the self-test, and a decoder is used to select steering multiplexers for implementing the spare column in regard to claim 8

(e.g.; column 9, lines 11 et seq; column 10, lines 1-3; figure 3);

During the second pass of self-test, the FAR stores unique failing row addresses, and at the end of the second pass of self-test, the FAR values are used to allocate and implement the spare rows in regard to claim 9

(e.g.; column 9, lines 63 et seq; column 10, lines 1-3; figure 3);

A BIST generates a column address signal designating a particular column in memory to be selected and tested, which is input to a first register which, which during BIST column testing, outputs the column address signal through a multiplexer to a decoder to select the particular column to be tested, the first register also outputs the worst tested column address signal to a second repair register, and during normal operation of the RAM the second repair register outputs the stored worst column address through the multiplexer to said decoder to implement the redundant data column in place of the worst tested column in regard to claim 10

(e.g.; column 9, lines 11 et seq; column 10, lines 1-3; figure 3);

In wide RAMs, RAM is divided into sections of adjacent columns, with each section having its own redundant column to replace a worst failing column in that section, and each section is tested in parallel with other sections of columns in regard to claim 14

(e.g.; column 11, lines 24-31);

The number of unique failing row addresses in two columns exceeds the number of redundant rows in a RAM, the RAM is designated as unrepairable in regard to claim 15

(e.g.; column 10, lines 30-46; figure 3);

And a method for self-testing, allocating and repairing a RAM using spare column and spare rows, performed on an embedded RAM within a microprocessor or logic chip in regard to claim 16

(e.g.; column 10, lines 49-51).

Allowable Subject Matter

3 The following is an examiner's statement of reasons for allowance:

Claim 2 recites, in part, "after completion of the second pass of self-test, transporting the failing column and unique failing row addresses to e-fuse macros for permanent storage in the RAM memory". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 11 recites, in part, "during the first pass of self-test, all columns except a selected tested column are masked or deselected such that only the un-masked selected column can produce an error in a data-out comparator, and a pass/fail signal from the data-out comparator is used to enable a Failing Address Register (FAR) to store each unique failing row address, and a counter is enabled to count the number of unique failing row addresses for the unmasked column". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 12 recites, in part, "at the end of testing of the unmasked column, if the count value for the unmasked column exceeds a previously stored worst count value from previously tested columns, then the unmasked column is determined to be the worst column so far, the count value for the unmasked column is stored in an error count register, and a bit-address for the unmasked data column is stored in a repair register". This feature in combination with the remaining claimed structure avoids the prior art of record.

Claim 13 recites, in part, "after testing of each unmasked column, the FAR and failing row counter are cleared before testing the next column, and the stored count value is subsequently compared to a count value for a next column after testing is completed on the next column, and at the completion of testing of all columns, the bit-address of worst column is stored and saved". This feature in combination with the remaining claimed structure avoids the prior art of record.

It is these limitations, which are not found, taught or suggested in the prior art of record, and are recited in the claimed combination that makes these claims allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas N Washburn whose telephone number is (571) 272-2284. The examiner can normally be reached on Monday through Thursday 6:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DNW

John Barlow
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